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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,142	09/17/2003	Stefano Sivcro	ATM-249	8212
3897	7590	09/26/2007	EXAMINER	
SCHNECK & SCHNECK			COX, CASSANDRA F	
P.O. BOX 2-E			ART UNIT	PAPER NUMBER
SAN JOSE, CA 95109-0005			2816	
			MAIL DATE	DELIVERY MODE
			09/26/2007	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

TH

**Office Action Summary**

Application No.

10/666,142

Applicant(s)

SIVERO ET AL.

Examiner

Cassandra Cox

Art Unit

2816

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --****Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION:

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 26 July 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 8-10 and 12-16 is/are allowed.
- 6) ☒ Claim(s) 1 is/are rejected.
- 7) ☒ Claim(s) 2-7 and 11 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date <u>12/18/03;12/23/03;7/26/05</u> | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Information Disclosure Statement***

1. The information disclosure statement filed 12/23/03 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

### ***Drawings***

2. Figure 1, 2A, 2B, 3A, 3B, and 4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### ***Claim Objections***

3. Claims 2, 7, and 11 are objected to because of the following informalities:

In line 17 of claim 2 after the term "second signal" insert the phrase --, and the third signal--.

In line 21 of claim 7 after the first occurrence of the word "signal" insert the phrase --, and the third signal--.

In line 35 of claim 11 after the first occurrence of the word "signal" insert the phrase --, and the third signal--.

Claims 7 and 11 are also objected to because they appear to disclose the level detector, first and second logic NOR gates, the set/reset latch, the first logic NAND gate and the third logic NOR gate as being in addition to the edge detector means rather than being a part of the edge detector means. The same applies to the pull-up and pull-down transistors with respect to the output driver means.

Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Pilling et al. (U.S. Patent No. 6,130,563).

In reference to claim 1, Pilling discloses in Figure 2 a circuit comprising an edge detector means (11-16) for sensing a rising edge and a falling edge of the clock signal ( $V_{IN}$ ) and generating respective pull-up and pull-down control signals in response thereto; and an output driver means (20, 21), connected to the edge

detector means (11-16) to receive the control signals therefrom, for recovering high and low logical levels of the clock signal ( $V_{IN}$ ).

***Allowable Subject Matter***

6. Claims 7-16 are allowed.
7. Claims 2-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
8. The following is a statement of reasons for the indication of allowable subject matter: Claims 2-5 would be allowable because the closest prior art of record fails to disclose an edge detector comprising a level detector means, a first logic NOR gate, a second logic Nor gate, a set/reset latch, a first logic NAND gate, and a third logic NOR gate in combination with the rest of the limitations of the base claims and any intervening claims. Claim 6 would be allowable because the closest prior art of record fails to disclose a circuit wherein the drain of the pull-up PMOS transistor is coupled to the drain of the NMOS pull-down transistor and to the clock signal in combination with the rest of the limitations of the base claims and any intervening claims.
9. The following is an examiner's statement of reasons for allowance: Claims 7-14 are allowed because the closest prior art of record fails to disclose an edge detector comprising a level detector means, a first logic NOR gate, a second logic Nor gate, a set/reset latch, a first logic NAND gate, and a third logic NOR gate in combination with the rest of the limitations of the base claims and any intervening claims. Claims 15-16 are allowed because the closest prior art of

record fails to disclose a method for regenerating a clock signal which includes generating a pull-up control signal in response to the detecting of the rise edge of the clock signal in combination with the rest of the limitations of the base claims and any intervening claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

#### ***Conclusion***

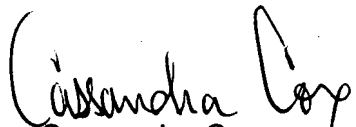
10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-1741. The examiner can normally be reached on Monday-Friday from 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on 571-272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

  
Cassandra Cox  
September 16, 2007